

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Sakae KOYATA et al.	Group Art Unit : 1792
Appl. No.	: 10/562,236	Examiner : Kin Chan Chen
Filed	: February 7, 2007	Confirmation No. : 3799
For	: MANUFACTURING METHOD OF SILICON WAFER	

**SUBMISSION OF SUPPLEMENTAL DECLARATION**

Commissioner for Patents  
U.S. Patent and Trademark Office  
Customer Service Window, Mail Stop **Issue Fee**  
Randolph Building  
401 Dulany Street  
Alexandria, VA 22314

Sir:

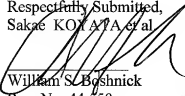
Applicants submit herewith an executed Declaration in support of the above-identified application, and supplemental to the executed Declaration filed on February 7, 2007.

Applicants respectfully request that this Supplemental Declaration, which include corrected foreign priority information and title, be made of record and entered into the prosecution file at the U.S. Patent and Trademark Office.

Authorization is hereby provided to charge and fee required for entry and/or consideration of this paper and the Supplemental Declaration to Deposit Account No. 19-0089.

Should there be any questions, please contact the undersigned at (703) 716-1191.

Respectfully Submitted,  
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